Confirmation No. 7385

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	BINK *et al.*	Examiner:	Petranek, J.
Serial No.:	10/598,583	Group Art Unit:	2183
Filed:	September 5, 2006	Docket No.:	NL040236US1 (NXPS.583PA)
Title:	ELECTRONIC CIRCUIT FOR REDUCING PIPELINE STAGES DEPENDENT UPON INSTRUCTIONS BEING EXECUTED		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed December 18, 2009 and in response to the rejections of claims 1-20 as set forth in the Final Office Action dated September 29, 2009.

Please charge Deposit Account No. 50-4019 (NL040236US1) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-20 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated September 29, 2009.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to an electronic circuit adapted to process a plurality of types of instruction, the electronic circuit (*see, e.g.*, pipeline 20 shown in Fig. 2, and page 4:15-20)

comprising: first and second pipeline stages, each of the first and second pipeline stages generating pipeline data (*see, e.g.*, pipeline stages 26 and 30 shown in Fig. 2, and page 4:21-34); a latch positioned between the first and second pipeline stages (*see, e.g.*, latch 28 shown in Fig. 2, and page 4:21-34); and wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal, through the latch (*see, e.g.*, page 6:6 to page 7:23); and wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage (*see, e.g.*, page 6:6-30).

Commensurate with independent claim 13, an example embodiment of the present invention is directed to a method of operating an electronic circuit, the electronic circuit being adapted to process a plurality of types of instruction (*see, e.g.*, pipeline 20 shown in Fig. 2, and page 4:15-20), the electronic circuit comprising first and second pipeline stages (*see, e.g.*, pipeline stages 26 and 30 shown in Fig. 2, and page 4:21-34) and a latch positioned between the first and second pipeline stages (*see, e.g.*, latch 28 shown in Fig. 2, and page 4:21-34), the method comprising: controlling modes of the electronic circuit in response to a control signal that is based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the second type of instruction to propagate, independent of the enable signal, through the latch (*see, e.g.*, page 6:6 to page 7:23); wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage (*see, e.g.*, page 6:6-30).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) over Hennessy ("Computer Organization and Design: The Hardware/Software Interface") in view of Colwell (U.S. Patent No. 5,604,878).

VII. Argument

The § 103(a) Rejection Of Claims 1-20 Is Improper Because The Cited Combination Of References Does Not Correspond To The Claimed Invention And The Hennessy Reference Teaches Away From The Proposed Combination.

A. The § 103(a) Rejection Of Claims 1-20 Is Improper Because The Cited References Fail To Disclose A Latch That Is Held Open For Generated Pipeline Data To Propagate Through The Latch In A Reduced Mode.

The cited Hennessy reference, either alone or in combination with the '878 reference, does not teach a latch that is held open for generated pipeline data to propagate through the latch in a reduced mode as in the claimed invention. Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejection fails.

The record establishes this clear lack of correspondence. The Examiner has expressly acknowledged that the Hennessy reference does not teach that the MEM/WB stage (*i.e.,* the asserted latch) is bypassed in a reduced mode (*see, e.g.,* page 3 of the final Office Action dated September 29, 2009). The '878 reference also fails to teach such aspects of the claimed invention. For example, the '878 reference teaches bypassing a pipe extend buffer 60 in a manner that does not involve data propagating through the buffer 60. *See, e.g.,* Figure 3 and Col. 7:55-62. Instead, the data is routed without passing through the buffer 60 as is shown in Figure 3. As such, the Examiner fails to cite to any reference that teaches that a latch is held open for the generated pipeline data to propagate through the latch in the reduced mode, as claimed.

In an apparent recognition of the lack of correspondence, the Examiner asserts that one way "to allow for early retirement ... would be to allow the MEM/WB pipeline register to be keep open ...which allows for the ALU result to flow out of the MEM/WB pipeline

register (*see* page 12 of the final Office Action dated September 29, 2009). However, as the Examiner fails to cite to any reference that teaches keeping MEM/WB pipeline register open to allow data to propagate through the register, the rejection necessarily fails and must be withdrawn. Appellant further submits that the Examiner is improperly attempting to modify the Hennessy reference in a manner that is taught, not by the cited references, but by Appellant, in a blatantly improper hindsight reconstruction of the claimed invention using Appellant's disclosure as a template. *See, e.g.,* M.P.E.P. § 2142.

In view of the above, the § 103(a) rejection of claims 1-20 is improper and Appellant requests that it be reversed.

B. The § 103(a) Rejection Of Claims 1-20 Is Improper Because The Cited References Fail To Disclose An Electronic Circuit That Has A Reduced Mode Of Operation.

The cited references do not teach an electronic circuit that has a reduced mode of operation that includes a truncated passage that bypasses a processing stage of a pipeline (*e.g.,* a latch is held open for the generated pipeline data to propagate through the latch), as in the claimed invention. Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejection fails.

More specifically, the Examiner expressly acknowledges that the Hennessy reference does not teach operation in a reduced mode that bypasses a processing stage of a pipeline (*see, e.g.,* page 3 of the final Office Action dated September 29, 2009). The '878 reference also fails to teach a reduced mode that bypasses a processing stage of a pipeline. Instead, the '878 reference teaches that a pipe extend buffer 60 is added after the end of the third pipe stage 43 of the unit. *See, e.g.,* Figure 3. The '878 reference uses the buffer 60 to extend the length of the pipeline when writeback conflict exists. *See, e.g.,* Col. 7:55-66. As such, the '878 reference teaches a normal mode and an extended mode, and the '878 reference fails to teach a reduced mode of operation, which involves such a latch being held open for pipeline processing as claimed. The Examiner generally and without explanation or supporting rationale asserts that the '878 reference teaches a reduced mode of operation, but no such mode is taught by the '878 reference as discussed above. Accordingly, the Examiner fails to

cite to any reference that discloses an electronic circuit that has a reduced mode of operation as in the claimed invention.

In view of the above, the § 103(a) rejection of claims 1-20 is improper and Appellant requests that it be reversed.

C. The § 103(a) Rejection Of Claims 2 and 3 is Improper Because The Cited References Fail To Disclose A Latch Control Circuit Configured To Provide An Enable Signal.

The cited references do not teach a latch control circuit configured to provide an enable signal to a latch in a normal mode and to prevent the enable signal from being provided to the latch in a reduced mode, as in the claimed invention. Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejection fails.

More specifically, the Examiner expressly acknowledges that the Hennessy reference does not teach operation in a reduced mode (*see, e.g.,* page 3 of the final Office Action dated September 29, 2009); as such, Appellant submits that Hennessy further does not teach a latch control circuit that prevents the enable signal from being provided to the latch in an apparently nonexistent reduced mode. The '878 reference also fails to teach such aspects of the claimed invention. For example, the '878 reference does not teach that control logic 60 (*i.e.,* the asserted latch control circuit) provides any signals to buffer 60. Instead, the control logic 62 provides a control signal to MUX 61 to select the desired output. *See, e.g.,* Figure 3. As such, the control logic 60 of the '878 reference does not provide an enable signal, or prevent the enable signal from being provided, to a pipeline stage (*e.g.,* the claimed latch). According to M.P.E.P. § 2111, claim terms must be interpreted in a manner consistent with Appellant's specification. In this instance, the Examiner fails to cite any reference that teaches a latch control circuit in a manner that is consistent with that disclosed and claimed by Appellant.

In view of the above, the § 103(a) rejection of claims 2 and 3 is improper and Appellant requests that it be reversed.

D. The § 103(a) Rejection Of Claims 1-20 Is Improper Because The Hennessy Reference Teaches Away From The Proposed Combination.

The Hennessy reference teaches away from the Examiner's proposed combination, which would undermine the operation of Hennessy. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a §103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main (Hennessy) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.").

In this instance, the Examiner proposes to modify the Hennessy reference such that MUX 61 and control logic 62 of the '878 reference (*see* Figure 3) are used to bypass MEM/WB stage of Hennessy's pipelined datapath (*see* Figure 6.25). However, as asserted by the Examiner, Hennessy is directed to a synchronous pipeline processor with each stage of the pipeline being controlled by a clock signal (*see* page 3:9-11 of the Final Office Action dated September 29, 2009). In particular, the Examiner states that the clock signal of the MEM/WB stage is overridden to allow data to bypass the MEM/WB stage (*see* page 4:14-16 of the Final Office Action dated September 29, 2009). However, Appellant submits that bypassing the MEM/WB stage (asserted by the Examiner to be a latch) would result in the corruption of the data being processed by Hennessy's synchronous pipeline processor. Specifically, bypassing the MEM/WB stage would result in the data output by the pipeline stage prior to the MEM/WB stage being passed through the MEM/WB stage to the pipeline stage after the MEM/WB stage prior to the receipt of the next pulse of the clock signal. As such, the input data to the pipeline stage after the MEM/WB stage would change before that stage finishes processing the current data, thereby resulting in the corruption of data being processed by the pipeline stage after the MEM/WB stage. Thus, the Hennessy reference requires the MEM/WB stage to ensure that data is not input to the pipeline stage after the MEM/WB stage too soon and thereby to maintain synchronization and avoid data corruption. Accordingly, the Examiner's proposed modification of bypassing the MEM/WB stage of Hennessy's pipeline would undermine the operation of the Hennessy reference.

In response to Appellant's previous arguments regarding the impropriety of the proposed modification of Hennessy, the Examiner mischaracterizes the teachings of the '878 reference in a failed attempt to maintain the rejection. Specifically, the Examiner erroneously asserts that "(w)hen the ALU instruction reaches the fourth pipeline stage, the control logic of Colwell [the '878 reference] determines that no conflict occurs in the fifth pipeline stage and that the ALU instruction can wire its data a clock cycle early to the register file" (*see* page 11 of the Final Office Action dated September 29, 2009). The '878 reference, however, does not teach that the control logic 62 allows for bypassing pipeline stages in the middle of Hennessey's synchronous pipeline processor. Instead, the '878 reference teaches that a pipe extend buffer 60 is added after the end of the third pipe stage 43 of the unit to extend the pipeline. *See, e.g.,* Figure 3. The '878 reference uses the buffer 60 and the control logic 62 to extend the length of the pipeline when writeback conflict exists. *See, e.g.,* Col. 7:55-66. As such, the '878 reference's control logic 62 does not make a determination that would allow for bypassing the MEM/WB stage in the middle of Hennessey's synchronous pipeline processor. Accordingly, the proposed combination does not address the fact that bypassing the MEM/WB stage of Hennessy's pipeline results in the corruption of the data being processed by Hennessy's synchronous pipeline processor, as discussed above. Thus, the Examiner's proposed modification would undermine the operation of the Hennessy reference.

In view of the above, the Hennessy reference teaches away from the Examiner's proposed modification and there is no motivation for the skilled artisan to modify Hennessy in such a manner. Accordingly, the § 103(a) rejection of claims 1-20 is improper and Appellant requests that it be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-20 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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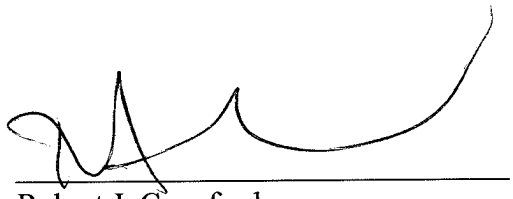
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/598,583)

1. An electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages, each of the first and second pipeline stages generating pipeline data;

a latch positioned between the first and second pipeline stages; and

wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal, through the latch; and

wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

2. The electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit configured to provide the enable signal to the latch to control the latch with the enable signal when the electronic circuit is in the normal mode, and configured to hold the latch open by preventing the enable signal from being provided to the latch when the electronic circuit is in the reduced mode.

3. The electronic circuit as claimed in claim 2, wherein the latch control circuit receives the control signal indicating whether the electronic circuit operates in the normal mode or in the reduced mode.

4. The electronic circuit as claimed in claim 1, wherein the electronic circuit is adapted to process a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage.

5. The electronic circuit as claimed in 4, wherein the electronic circuit is adapted to operate in the normal mode until an instruction of the third type of instruction is processed.

6. The electronic circuit as claimed in claim 5, wherein, after the instruction of the third type of instruction is processed, the electronic circuit is adapted to operate in the reduced mode if an instruction, following the instruction of the third type of instruction, is of the second type of instruction or the third type of instruction.

7. The electronic circuit as claimed in claim 4, wherein the electronic circuit is adapted to operate in the reduced mode until an instruction of the first type of instruction is processed.

8. The electronic circuit as claimed in claim 1, wherein the first type of instruction includes a load instruction, and wherein the first and second pipeline stages are asynchronous pipeline stages that are each controlled responsive to different enable signals.

9. The electronic circuit as claimed in claim 1, wherein the second type of instruction includes an arithmetic computation instruction.

10. The electronic circuit as claimed in claim 4, wherein the third type of instruction includes compare, store, branch and jump instructions.

11. The electronic circuit as claimed in claim 1, wherein the first pipeline stage comprises a data memory.

12. The electronic circuit as claimed in any claim 1, wherein the second pipeline stage comprises a write back stage.

13. A method of operating an electronic circuit, the electronic circuit being adapted to process a plurality of types of instruction, the electronic circuit comprising first and second pipeline stages and a latch positioned between the first and second pipeline stages, the method comprising:

controlling modes of the electronic circuit in response to a control signal that is based on a latency period of each respective instruction of said plurality of types of instruction, said electronic circuit being in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal, and a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the second type of instruction to propagate, independent of the enable signal, through the latch; wherein the first type of instruction requires processing by the first and second pipeline stages and the second type of instruction requires processing by the second pipeline stage.

14. The method as claimed in claim 13, wherein controlling the electronic circuit further includes processing a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage.

15. The method as claimed in claim 14, further comprising operating the electronic circuit in the normal mode until an instruction of the third type of instruction is processed.

16. The method as claimed in claim 15, wherein, after processing the instruction of the third type of instruction, the method further comprises operating the electronic circuit in the reduced mode if an instruction, following the instruction of the third type of instruction, is of the second type of instruction or the third type of instruction.

17. The method as claimed in claim 14, further comprising operating the electronic circuit in the reduced mode until an instruction of the first type of instruction is processed.

18. The method as claimed in claim 13, wherein the first type of instruction includes a load instruction, and wherein the enable signal is provided to the latch in the normal mode to open and close the latch, and the control signal prevents the enable signal from being provided to the latch in the reduced mode.

19. The method as claimed in claim 13, wherein the second type of instruction includes an arithmetic computation instruction, and wherein the first and second pipeline stages are asynchronous pipeline stages that are each controlled responsive to different enable signals.

20. The method as claimed in claim 14, wherein the third type of instruction includes compare, store, branch and jump instructions.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.